

## 1. INTRODUCTION

CT48248NS126A-xxxx-x is a Multi Chip Package Memory (MCP) that integrated 1G bits NAND Flash and 512M bits DDR2 SDRAM by advanced SiP (System-in-a-Package) technology. CT48248NS126A-xxxx-x offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

### 1.1 APPLICATION

- DSC
- DV
- PMP

### 1.2 FEATURES

#### PRODUCT LIST

- CT48248NS126A-xxxx-x
  - NAND FLASH: 1G bits (128Mx8-bit)
  - DDR2 SDRAM: 512M bits (8M x4-Bank x16-bit)

#### POWER SUPPLY

- NAND FLASH
  - 3.3V
- DDR2 SDRAM
  - 1.8V

#### PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- FBGA 9.0 x 9.0 x 1.2mm, 104 Balls
- Ball Pitch: 0.65 mm
- Weight:0.17g

#### Temperature

- Operating: 0 to +70 °C
- Storage: -55 to +125 °C

#### NAND FLASH

- Voltage Supply
  - 3.3V Device : 2.70V ~ 3.60V
- Organization
  - Memory Cell Array : (128M + 4M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (128K + 4K)Byte
- Page Read Operation
  - Page Size : (2K + 64)Byte
  - Random Read : 25µs(Max.)

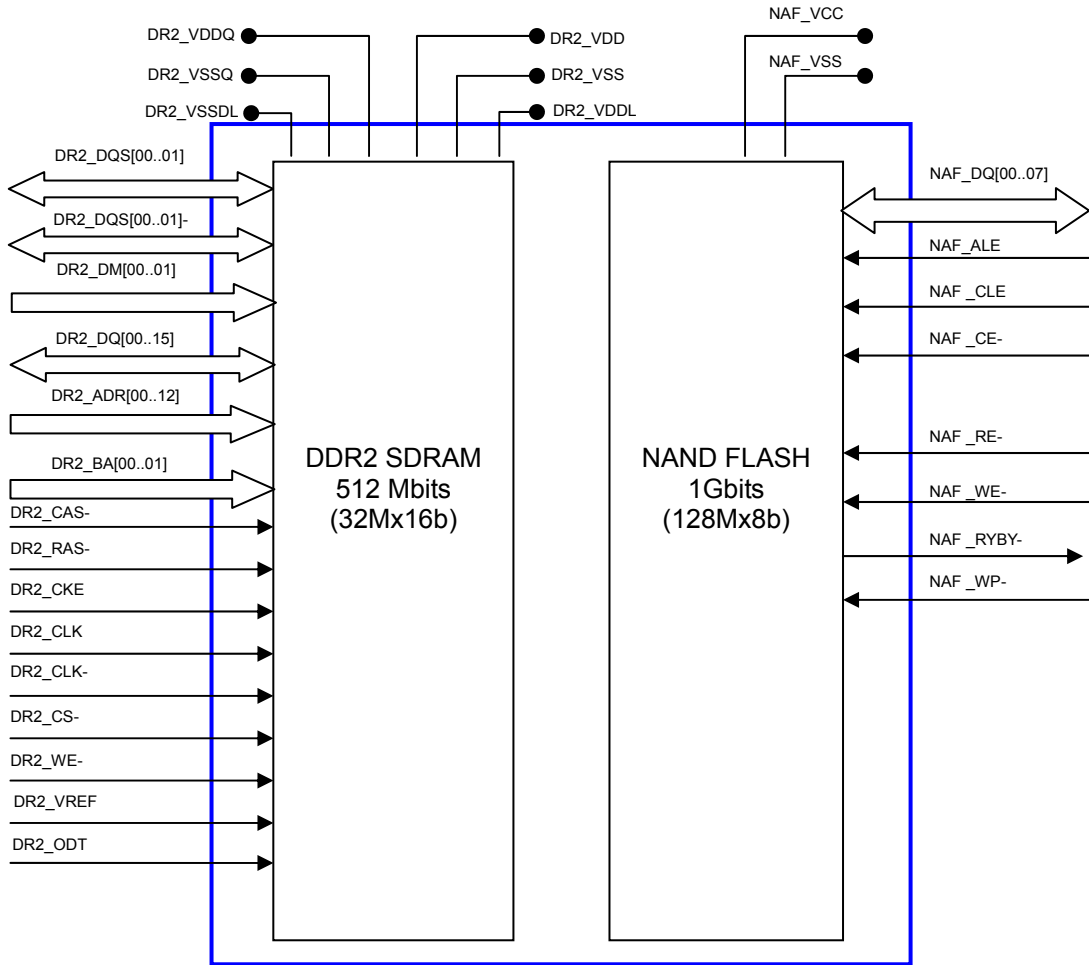
- Serial Access : 25ns(Min.)
- Fast Write Cycle Time
  - Page Program time : 200µs(typ.)
  - Block Erase Time : 1.5ms(typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles(with 1bit/512Byte ECC)
  - Data Retention : 10 Years
- Command Driven Operation
- Intelligent Copy-Back with internal 1bit/528Byte EDC

#### DDR2 SDRAM

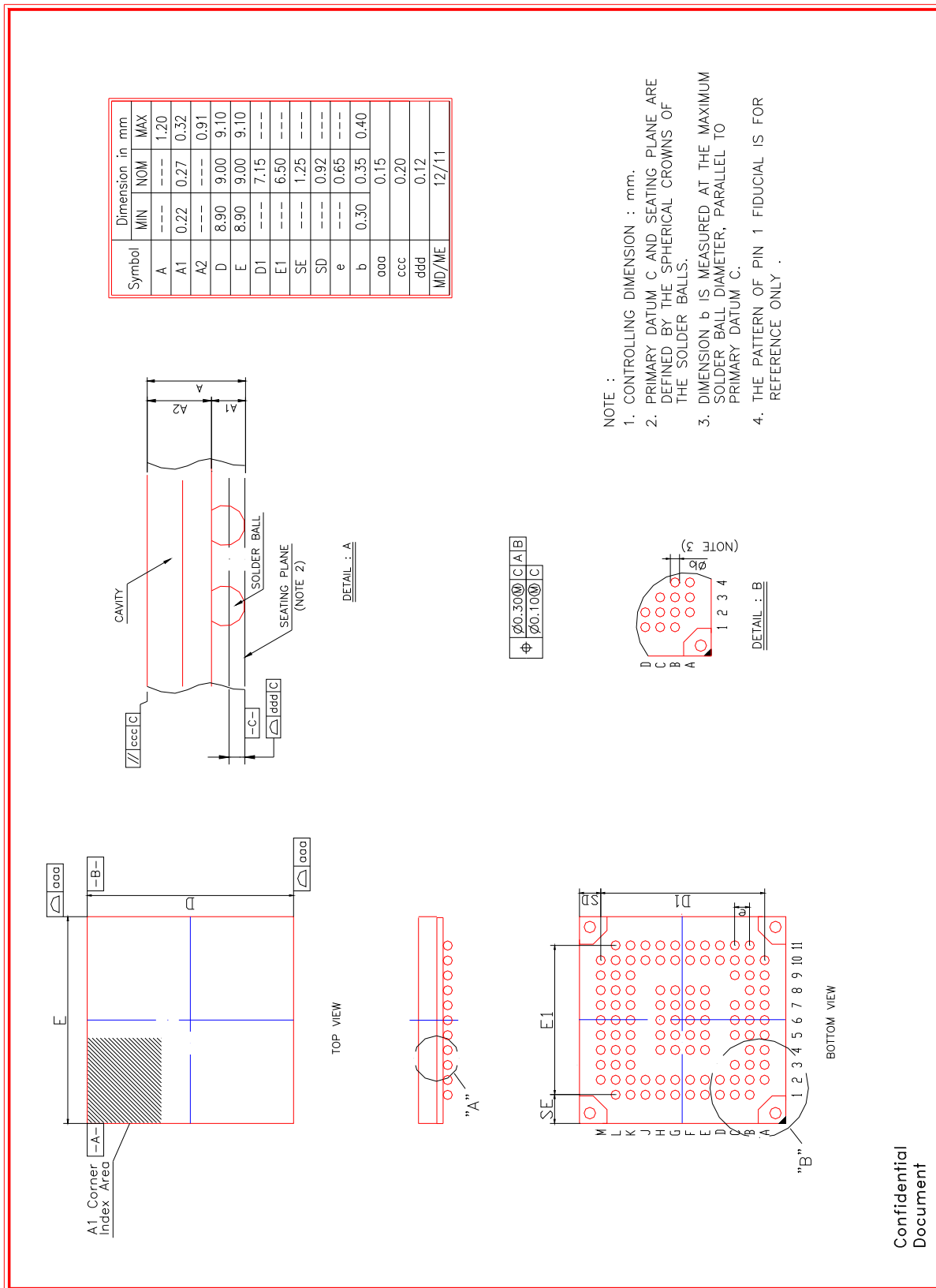
- JEDEC standard DR2\_VDD = 1.8V ± 0.1V Power Supply
- DR2\_VDDQ = 1.8V ± 0.1V
- 333MHz fck for 667Mb/sec/pin
- 4 Banks
- Posted DR2\_CAS-
- Programmable DR2\_CAS- Latency: 3, 4, 5, 6
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended datastrobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Special Function Support
  - 50ohm ODT
  - High Temperature Self-Refresh rate enable

**2. FUNCTION DIAGRAM**

**2.1 MCP**



**3. PACKAGE DIMENSION (104 Ball FBGA, 9x9x1.2mm)**



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