

## 1. INTRODUCTION

CT48248NS246C-xxxx-x is a Multi Chip Package Memory (MCP) that integrated 1G bits NAND Flash and 1G bits DDR2 SDRAM by advanced SiP (System-in-a-Package) technology. CT48248NS246C-xxxx-x offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

### 1.1 APPLICATION

- DSC
- DV
- PMP

### 1.2 FEATURES

#### PRODUCT LIST

- CT48248NS246C-xxxx-x
  - NAND FLASH: 1G bits (128Mx8bit)
  - DDR2 SDRAM: 1G bits (8M x8-Bank x 16-bit)

#### POWER SUPPLY

- NAND FLASH
  - 3.3V
- DDR2 SDRAM
  - 1.8V

#### PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- FBGA 10.0 x 13.0 x 1.2mm, 119 Balls
- Ball Pitch: 0.8 mm
- Weight:0.27g

#### Temperature

- Operating: 0 to +70 °C
- Storage: -55 to +125 °C

#### NAND FLASH

- Voltage Supply
  - 3.3V Device : 2.70V ~ 3.60V
- Organization
  - Memory Cell Array : (128M + 4M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (128K + 4K)Byte
- Page Read Operation
  - Page Size : (2K + 64)Byte
  - Random Read : 25µs(Max.)
  - Serial Access : 25ns(Min.)
- Fast Write Cycle Time
  - Page Program time : 200µs(typ.)
  - Block Erase Time : 1.5ms(typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology

- Endurance : 100K Program/Erase Cycles(with 1bit/512Byte ECC)
- Data Retention : 10 Years

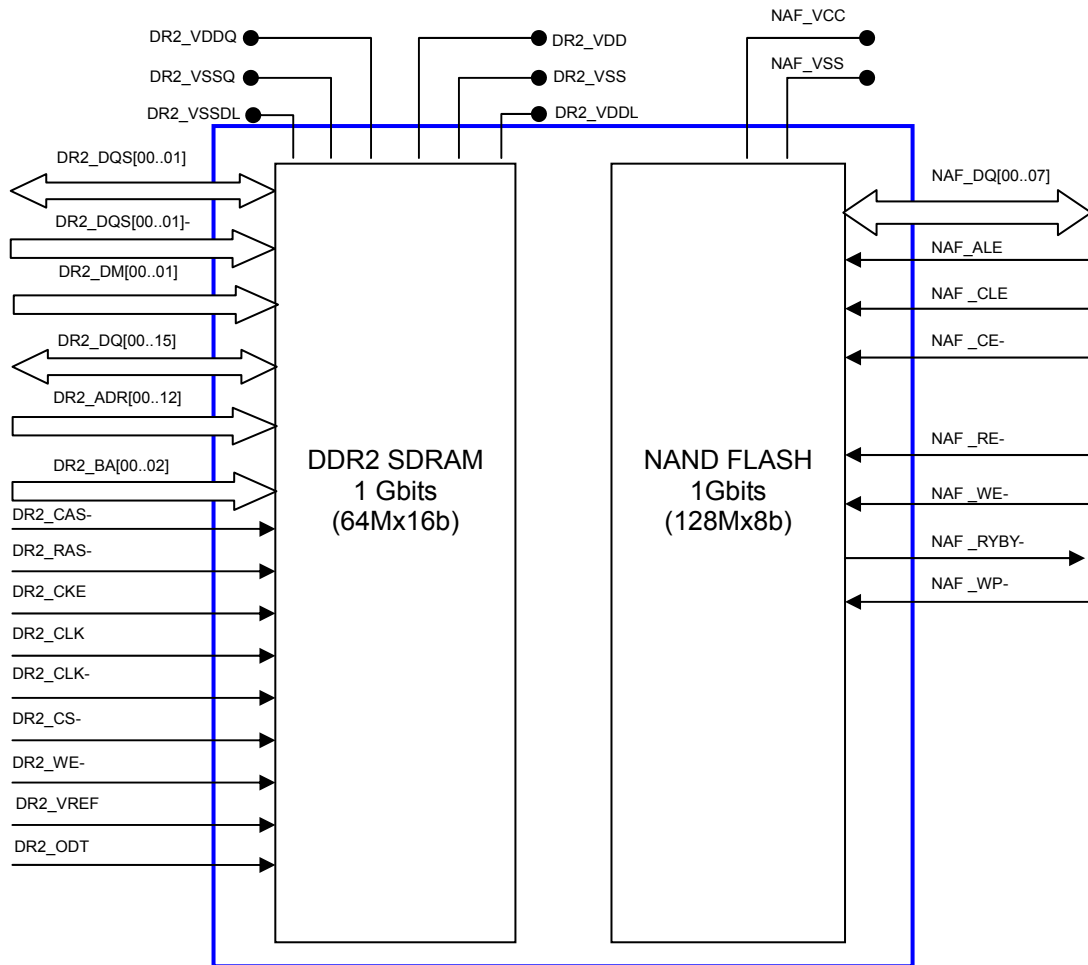
- Command Driven Operation
- Intelligent Copy-Back with internal 1bit/528Byte EDC

#### DDR2 SDRAM

- DR2\_VDD = 1.8 +/- 0.1V
- DR2\_VDDQ = 1.8 +/- 0.1V
- All inputs and outputs are compatible with SSTL\_18 interface
- 8 banks
- Fully differential clock inputs (DR2\_CLK, /DR2\_CLK-) operation
- Double data rate interface
- Source synchronous-data transaction aligned to bidirectional data strobe (DR2\_DQS[00..01], DR2\_DQS[00..01]-)
- Differential Data Strobe (DR2\_DQS[00..01], DR2\_DQS[00..01]-)
- Data outputs on DR2\_DQS[00..01], DR2\_DQS[00..01]- edges when read (edged DR2\_DQ[00..15])
- Data inputs on DR2\_DQS[00..01] centers when write (centered DR2\_DQ[00..15])
- On chip DLL align DR2\_DQ[00..15], DR2\_DQS[00..01] and DR2\_DQS[00..15]- transition with DR2\_CLK transition
- DR2\_DM[00..01] mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable DR2\_CAS- latency 3, 4, 5 and 6 supported
- Programmable additive latency 0, 1, 2, 3, 4 and 5 supported
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- Internal eight bank operations with single pulsed DR2\_RAS
- Auto refresh and self refresh supported
- tRAS lockout supported
- 8K refresh cycles /64ms
- Full strength driver option controlled by EMR
- On Die Termination supported
- Off Chip Driver Impedance Adjustment supported
- Self-Refresh High Temperature Entry

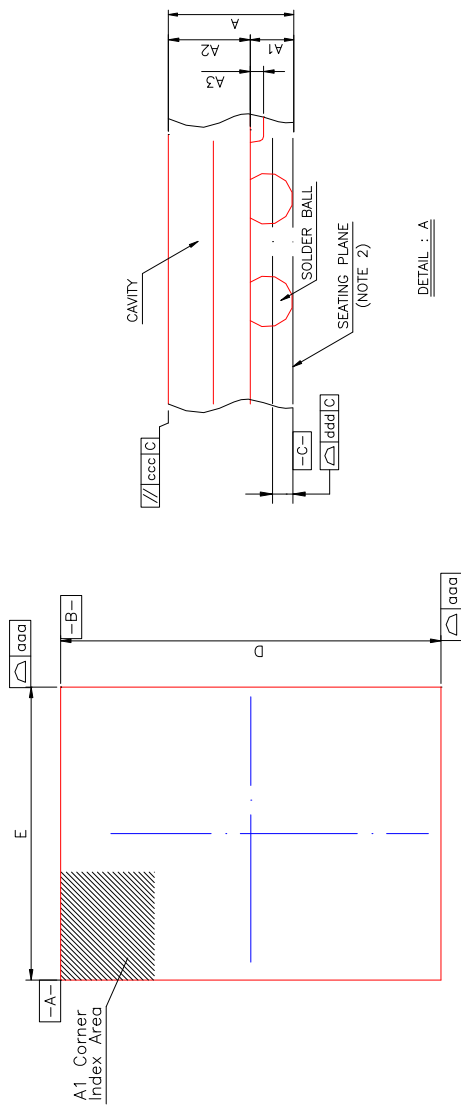
**2. FUNCTION DIAGRAM**

**2.1 MCP**

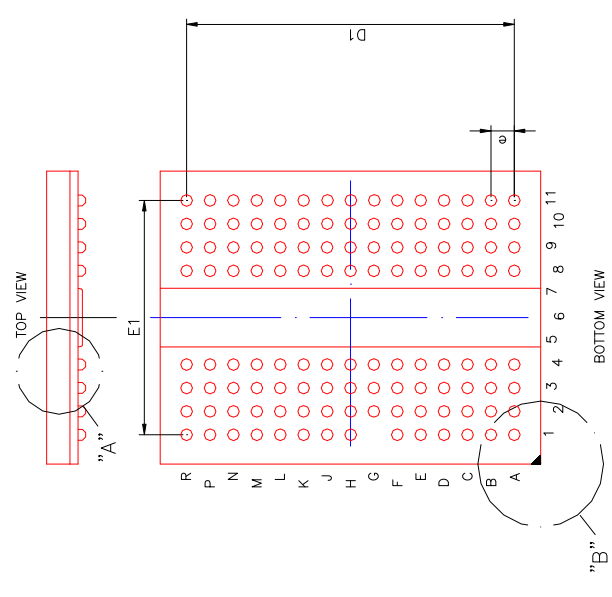


**3. PACKAGE DIMENSION (119 Ball FBGA, 10x13x1.2mm)**

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	1.20	1.30
A1	0.30	0.35	0.40
A2	---	---	0.96
A3	---	0.15	---
D	12.90	13.00	13.10
E	9.90	10.00	10.10
D1	---	11.20	---
E1	---	8.00	---
e	---	0.8	---
b	0.40	0.45	0.50
aaa	---	0.15	---
ccc	---	0.20	---
ddd	---	0.12	---
MD/ME	---	---	15/11



DETAIL : A



$\phi$  00.25 C A B  
 $\phi$  01.10 C

DETAIL : B

- NOTE :
1. CONTROLLING DIMENSION : mm.
  2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
  3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
  4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

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