

## 1. INTRODUCTION

CT48568SR126A-xxxx-x is a Multi Chip Package Memory (MCP) that integrated 256M bits NAND Flash and 512M bits DDR2 SDRAM by advanced SiP (System-in-a-Package) technology. CT48568SR126A-xxxx-x offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

### 1.1 APPLICATION

- DSC
- DV
- PMP

### 1.2 FEATURES

#### PRODUCT LIST

- CT48568SR126A-xxxx-x
  - NAND FLASH: 256M bits (32Mx8-bit)
  - DDR2 SDRAM: 512M bits (8Mx4-Bank x16-bit)

#### POWER SUPPLY

- NAND FLASH
  - 3V
- DDR2 SDRAM
  - 1.8V

#### PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- FBGA 9.0 x 9.0 x 1.2mm, 104 Balls
- Ball Pitch: 0.65 mm
- Weight:0.17g

#### Temperature

- Operating: 0 to +70 °C
- Storage: -55 to +125 °C

#### NAND FLASH

- HIGH DENSITY NAND FLASH MEMORIES
  - Up to 1 Gbit memory array
  - Up to 32 Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND INTERFACE
  - x8 bus width
  - Multiplexed Address/ Data
  - Pinout compatibility for all densities
- SUPPLY VOLTAGE
  - 3V device: NAF\_VCC = 2.7 to 3.6V
- PAGE SIZE
  - x8 device: (512 + 16 spare) Bytes
- BLOCK SIZE
  - x8 device: (16K + 512 spare) Bytes

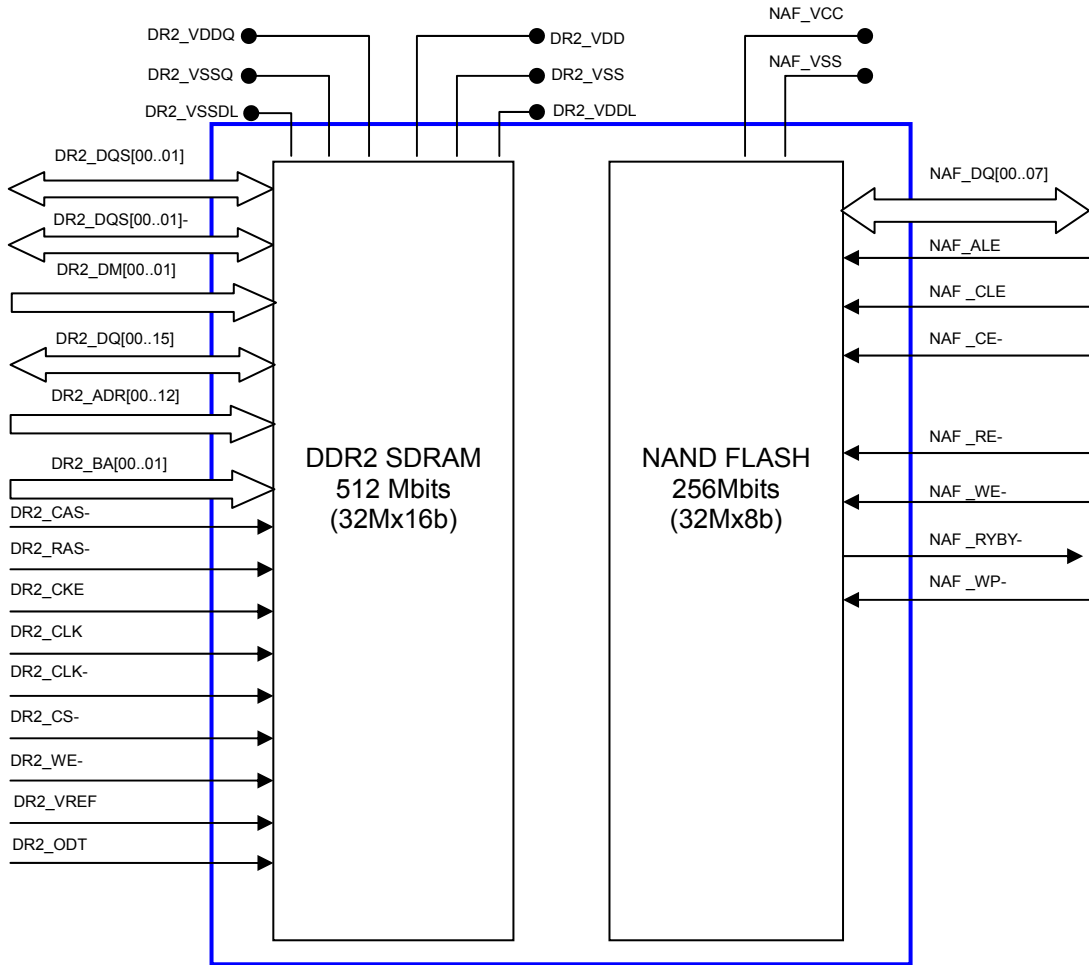
- PAGE READ / PROGRAM
  - Random access: 12µs (3V)
  - Sequential access: 50ns (min)
  - Page program time: 200µs (typ)
- COPY BACK PROGRAM MODE
  - Fast page copy without external buffering
- FAST BLOCK ERASE
  - Block erase time: 2ms (typ)
- STATUS REGISTER
- ELECTRONIC SIGNATURE
- CHIP ENABLE 'DON'T CARE'
  - Simple interface with microcontroller
- HARDWARE DATA PROTECTION
  - Program/Erase locked during Power transitions
- DATA INTEGRITY
  - 100,000 Program/Erase cycles
  - 10 years Data Retention

#### DDR2 SDRAM

- JEDEC standard DR2\_VDD = 1.8V ± 0.1V Power Supply
- DR2\_VDDQ = 1.8V ± 0.1V
- 333MHz fck for 667Mb/sec/pin
- 4 Banks
- Posted DR2\_CAS-
- Programmable DR2\_CAS- Latency: 3, 4, 5, 6
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended datastrobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Special Function Support
  - 50ohm ODT
  - High Temperature Self-Refresh rate enable

**2. FUNCTION DIAGRAM**

**2.1 MCP**



**3. PACKAGE DIMENSION (104 Ball FBGA, 9x9x1.2mm)**

