

1. INTRODUCTION

CT72646MT646- is a Multi Chip Package Memory (MCP) that integrated 64M bits NOR Flash and 64M bits SDRAM by advanced SiP (System-in-a-Package) technology. CT72646MT646 offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

1.1 APPLICATION

- Mobile Phone

1.2 FEATURES

PRODUCT LIST

- CT72646MT646
- NOR FLASH: 64M bits (4Mx 16bit)
- SDRAM: 64M bits (4M x 16bit)

POWER SUPPLY

- NOR FLASH
 - 1.8 V
- SDRAM
 - 3.0V

PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- TFBGA :8x 10 x 1.4mm, 125 Balls
- Ball Pitch: 0.65 mm

Temperature

- Operating: 0 to +70 °C
- Storage: -55 to +125 °C

NOR FLASH

- **High Performance Read-While-Write/Erase**
 - Burst frequency at 66 MHz (zero wait states)
 - 60 ns Initial access read speed
 - 11 ns Burst mode read speed
 - 20 ns Page mode read speed
 - 4-, 8-, 16-, and Continuous-Word Burst mode reads
 - Burst and Page mode reads in all Blocks, across all partition boundaries
 - Burst Suspend feature
 - Enhanced Factory Programming at 3.1 μ s/word
- **Security**
 - 128-bit OTP Protection Register:
64 unique pre-programmed bits +
64 user-programmable bits
 - Absolute Write Protection with VPP at ground
 - Individual and Instantaneous Block Locking/Unlocking with Lock-Down Capability

- **Quality and Reliability**

- 100K Erase Cycles per Block
- 90 nm ETOX™ IX Process

- **Architecture**

- Multiple 4-Mbit partitions
- Dual Operation: RWW or RWE
- Parameter block size = 4-Kword
- Main block size = 32-Kword
- Top or bottom parameter devices
- 16-bit wide data bus

- **Software**

- 5 μ s (typ.) Program and Erase Suspend latency time
- Flash Data Integrator (FDI) and Common Flash Interface (CFI) Compatible
- Programmable WAIT signal polarity

- **Packaging and Power**

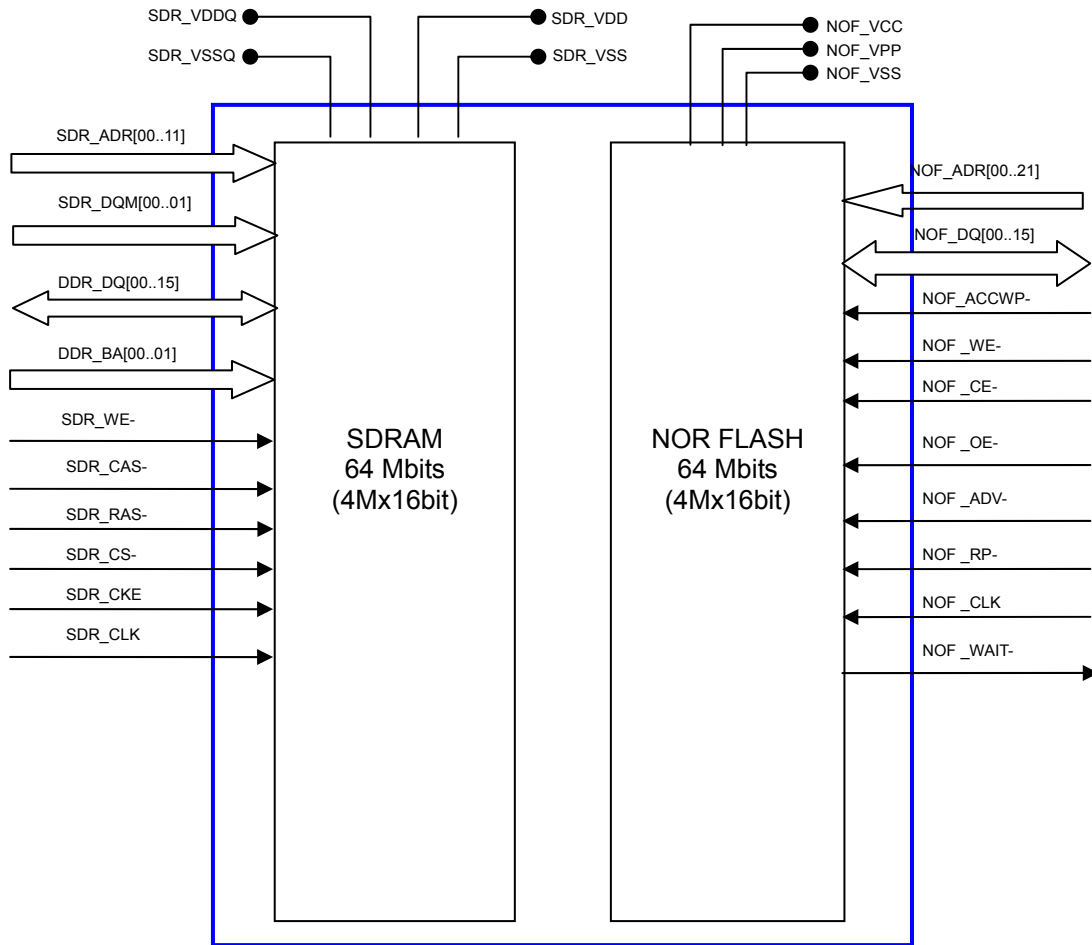
- 90 nm: 32- and 64-Mbit in FBGA
- NOF_VCC = 1.70 V to 1.95 V
- Read current: 8 mA (4-word burst, typ.)

SDRAM

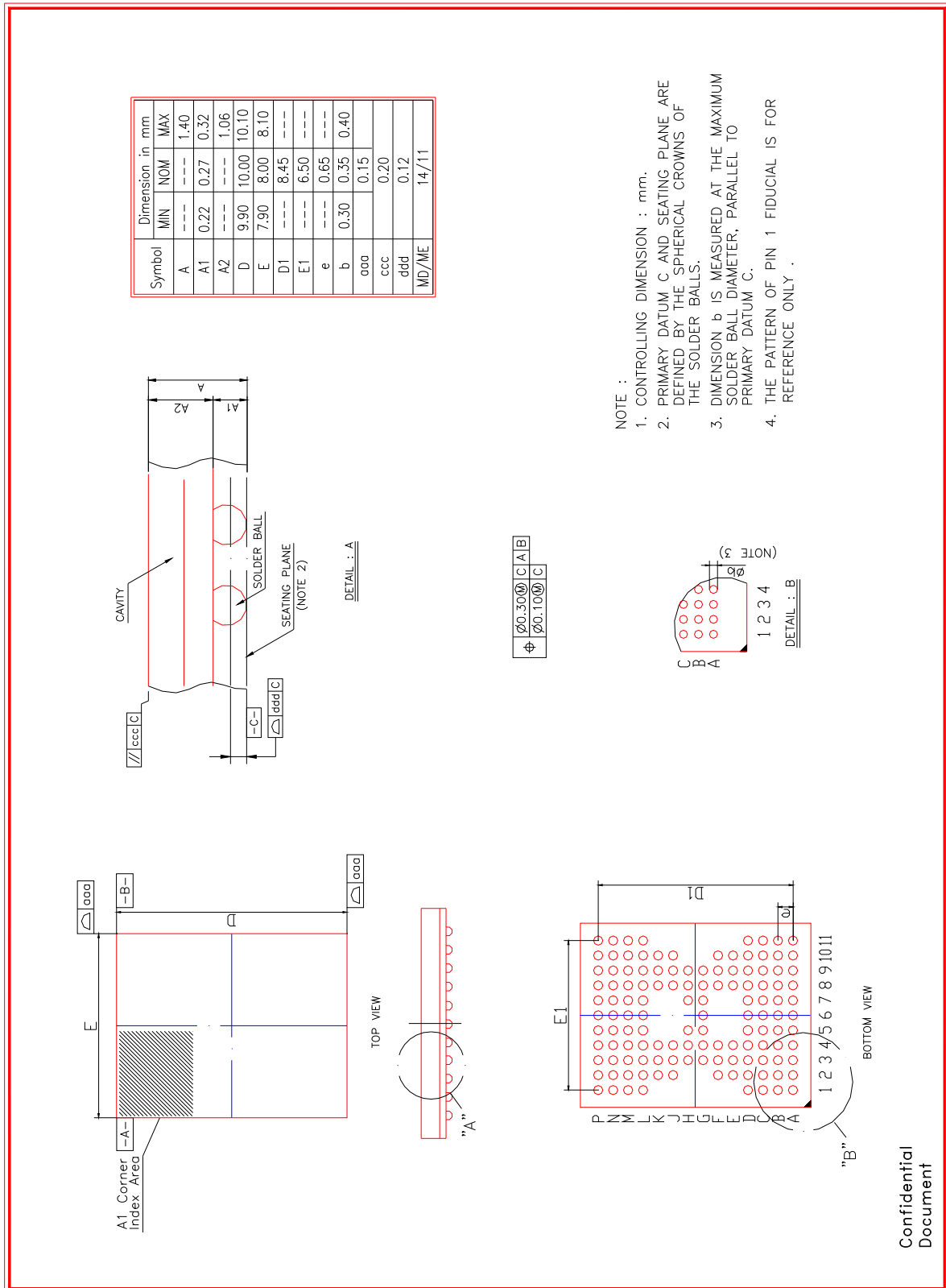
- 1M word \times 16 bit \times 4 banks organization
- Low power supply
 - SDR_VDD: +1.7 V to +1.95V
 - SDR_VDDQ: +1.7 V to +1.95V
- 1.8V-CMOS I/O interface
- 4 K refresh cycles every 64 ms
- Auto and Self-refresh
- Four banks operation
- Burst read/write operation and burst read/single write operation capability
- Programmable burst type, burst length and SDR_CAS Latency
- Programmable Partial Array Self Refresh (PASR)
- Programmable Driver Strength (DS)
- Deep power down mode
- SDR_CKE power down mode
- Output enable and input data mask

2. FUNCTION DIAGRAM

2.1 CT72646MT646



3. PACKAGE DIMENSION (125 Ball FBGA, 8x10x1.4mm)



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