

Brief Datasheet

PRODUCT: 2Gb DDR2 (x32) MCP

DESCRIPTION: Combo Memory (Green MCP)
DDR2 SDRAM 2Gb (x32)
Outline : 10.5x13.5x1.1 mm, Pitch : 0.8 mm, FBGA 128Balls

Approved Signatures	鉅景科技 股份有限公司
	Contact Person:

DOCUMENT TITLE

2Gb DDR2 (X32) MCP
2G bits DDR2 SDRAM
Green MCP memory product

REVISION HISTORY

VERSION	DATE	Total	Page	DESCRIPTION
Rev 0.1	2009/05/08	4	ALL	Create new document
Rev 0.2	2009/05/21	5	3	Modified: PIN CONFIGURATION
			4	Modified: PACKAGE DIMENSION
			0,2,5	Change package from 10x13 mm to 10.5x13.5 mm,137 Balls to 128 Balls
Rev 0.3	2009/05/21	5	4	<ol style="list-style-type: none">1. Add description " Page 3.11.4-44" under description of " JEDEC Standard No. 21-C".2. Move all ball names to the center of each ball section.3. Modify the typing error of name for ball J02 from " DR2_ADR03/AP" to " DR2_ADR10/AP".4. Modify H01 ball name from "NC. DR2_BA02" to " DR2_BA02".5. Modify K07 ball name from " NC. DR2_ADR13" to " NC".6. Add bottom line from ball T05 to T08.7. Remove the below description : "The pin configuration is for information only. ChipSiP Technology Co., Ltd. assumes no responsibility for errors or omissions and reserves the right to change without notice."
			5	<ol style="list-style-type: none">1. Modify the dimension of A3 on page 5 from "MIN/---, NOM/0.15, MAX/---" to "MIN/0 , NOM/--- , MAX/0.15"

1 INTRODUCTION

2Gb DDR2 (X32) MCP is a Multi Chip Package Memory (MCP) that integrated 1G bits x2 DDR2 SDRAM by advanced SiP (System-in-a-Package) technology. It offers space saving advantage that could miniaturize system board device and also conformed with Green regulations.

1.1 APPLICATION

- DSC, DSLR, Entertainment

1.2 FEATURE

Product List

- DDR2 SDRAM: 2G bits (64Mx32bit)

Power Supply

- 1.8V

Package

- Solder Ball Material : 96.5%Sn / 3%Ag / 0.5% Cu
- FBGA Dimensions : 10.5 x 13.5 x 1.1 mm
- Ball Counts : 128 Balls
- Ball Pitch : 0.8 mm
- Weight : TBD

Temperature

- Operating : 0 to +85 °C
- Storage : -55 to +100 °C

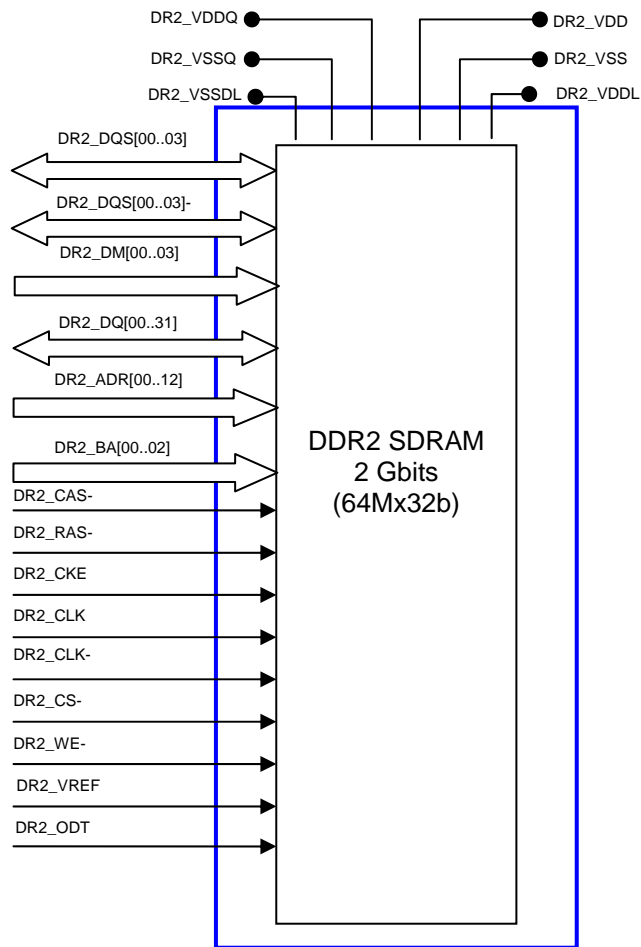
Speed Transfer Rates

- 667 Mb/sec (DDR2-667)

DDR2 SDRAM Features

- Power Supply : VDD, VDDQ = 1.8 V \pm 0.1 V
- Double Data Rate architecture : two data transfers per clock cycle
- CAS Latency supported
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DQS and DQS-) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLK-)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Posted CAS- programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

2. FUNCTION DIAGRAM



3. PIN CONFIGURATION

JEDEC Standard No.21-C

Page 3.11.4-44

DDR2x32 SDRAM Ball Out

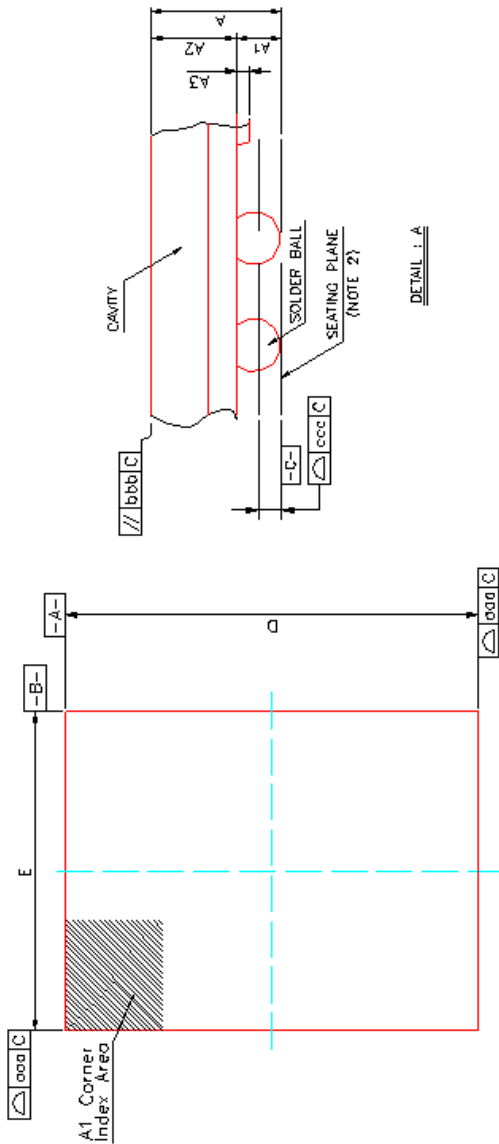
	01	02	03	04	05	06	07	08	09	10	11	12
A	DR2_VDD	DR2_DQ00	DR2_VSSQ	DR2_VSS	X	X	X	X	DR2_VSS	DR2_VSSQ	DR2_DQ08	DR2_VDD
B	DR2_DQ01	DR2_VDDQ	DR2_DQ02	DR2_VDDQ	X	X	X	X	DR2_VDDQ	DR2_DQ10	DR2_VDDQ	DR2_DQ09
C	DR2_VSSQ	DR2_DQ03	DR2_VSSQ	DR2_DQS00-	X	X	X	X	DR2_DQS01-	DR2_VSSQ	DR2_DQ11	DR2_VSSQ
D	DR2_DQ04	DR2_VDDQ	DR2_DQS00	DR2_VDDQ	X	X	X	X	DR2_VDDQ	DR2_DQS01	DR2_VDDQ	DR2_DQ12
E	DR2_VSSQ	DR2_DQ05	DR2_VSSQ	DR2_DQ06	X	X	X	X	DR2_DQ14	DR2_VSSQ	DR2_DQ13	DR2_VSSQ
F	DR2_DQ07	DR2_VDDQ	DR2_DM00	DR2_VSS	X	X	X	X	DR2_VDDQ	DR2_DM01	DR2_VDDQ	DR2_DQ15
G	DR2_WE-	DR2_VREF	DR2_CKE	DR2_BA00	X	X	X	X	DR2_RAS-	DR2_CAS-	DR2_ODT	DR2_CLK
H	DR2_BA02	DR2_BA01	DR2_VDD	DR2_VDDL	X	X	X	X	DR2_VSSL	DR2_VSS	DR2_CS-	DR2_CLK-
J	DR2_ADR03	DR2_ADR10/ AP	DR2_ADR01	DR2_ADR07	X	X	X	X	DR2_ADR02	DR2_ADR00	DR2_ADR06	DR2_ADR04
K	DR2_VDD	DR2_ADR09	DR2_ADR05	DR2_ADR12	X	X	X	X	NC	DR2_ADR11	DR2_ADR08	DR2_VSS
L	DR2_DQ23	DR2_VDDQ	DR2_DM02	DR2_VSS	X	X	X	X	DR2_VDDQ	DR2_DM03	DR2_VDDQ	DR2_DQ31
M	DR2_VSSQ	DR2_DQ21	DR2_VSSQ	DR2_DQ22	X	X	X	X	DR2_DQ30	DR2_VSSQ	DR2_DQ29	DR2_VSSQ
N	DR2_DQ20	DR2_VDDQ	DR2_DQS02	DR2_VDDQ	X	X	X	X	DR2_VDDQ	DR2_DQS03	DR2_VDDQ	DR2_DQ28
P	DR2_VSSQ	DR2_DQ19	DR2_VSSQ	DR2_DQS02-	X	X	X	X	DR2_DQS03-	DR2_VSSQ	DR2_DQ27	DR2_VSSQ
R	DR2_DQ17	DR2_VDDQ	DR2_DQ18	DR2_VDDQ	X	X	X	X	DR2_VDDQ	DR2_DQ26	DR2_VDDQ	DR2_DQ25
T	DR2_VDD	DR2_DQ16	DR2_VSSQ	DR2_VSS	X	X	X	X	DR2_VSS	DR2_VSSQ	DR2_DQ24	DR2_VDD

Package : MO-210
Ball Pitch=0.8mm

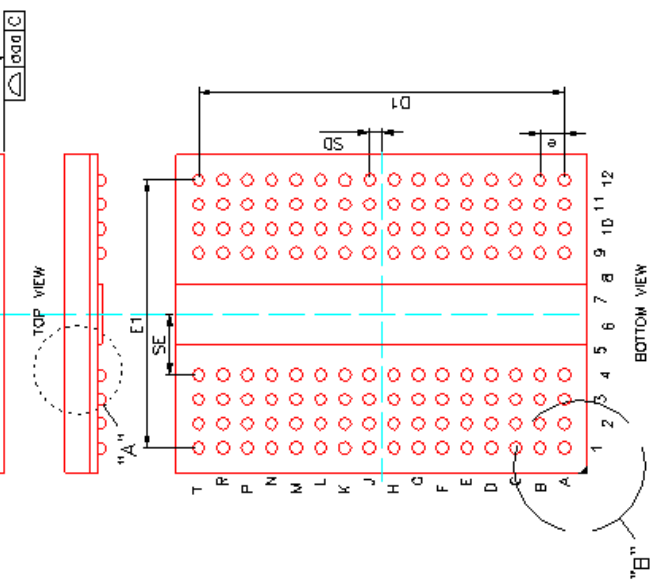
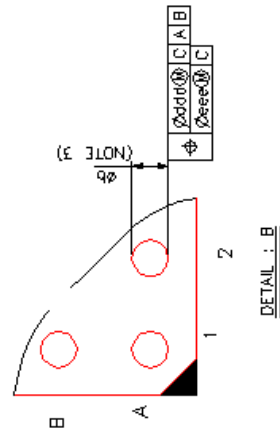
TOP VIEW

4. PACKAGE DIMENSION (128 Ball FBGA, 10.5x13.5x1.1 mm)

Symbol	Dimension in mm	
	MIN	NOM MAX
A	---	1.10
A1	0.30	0.35 0.40
A2	---	0.75
A3	0	0.15
D	13.40	13.50 13.60
E	10.40	10.50 10.60
D1	---	12.00
E1	---	8.80
e	---	0.8
b	0.40	0.45 0.50
SD	---	0.40
SE	---	0.40
ooo	---	0.15
bbb	---	0.20
ccc	---	0.12
ddd	---	0.12
eee	---	0.08
MD/ME	---	16/12



- NOTE :
1. CONTROLLING DIMENSION : mm.
 2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .



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