

## 1. INTRODUCTION

M5E1G81G2B is a Multi Chip Package Memory (MCP) that integrated 1G bits NAND Flash and 1G bits Mobile DDR SDRAM by advanced SiP (System-in-a-Package) technology. M5E1G81G2B offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

## 1.1 APPLICATION

- Feature Phone
- Smart Phone
- MID

## 1.2 FEATURE

### PRODUCT LIST

- M5E1G81G2B
  - NAND FLASH: 1G bits (128Mx8bit)
  - Mobile DDR SDRAM: 1G bits (8Mx32bit x4-Bank)

### POWER SUPPLY

- NAND FLASH
  - 2.7 to 3.6V
- MOBILE DDR SDRAM
  - 1.8V

### PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- FBGA11 x 13 x 1.2mm, 137 Balls
- Ball Pitch: 0.8 mm

### Temperature

- Operating: 0 to +70 °C
- Storage: -65 to +150 °C

### NAND FLASH Features

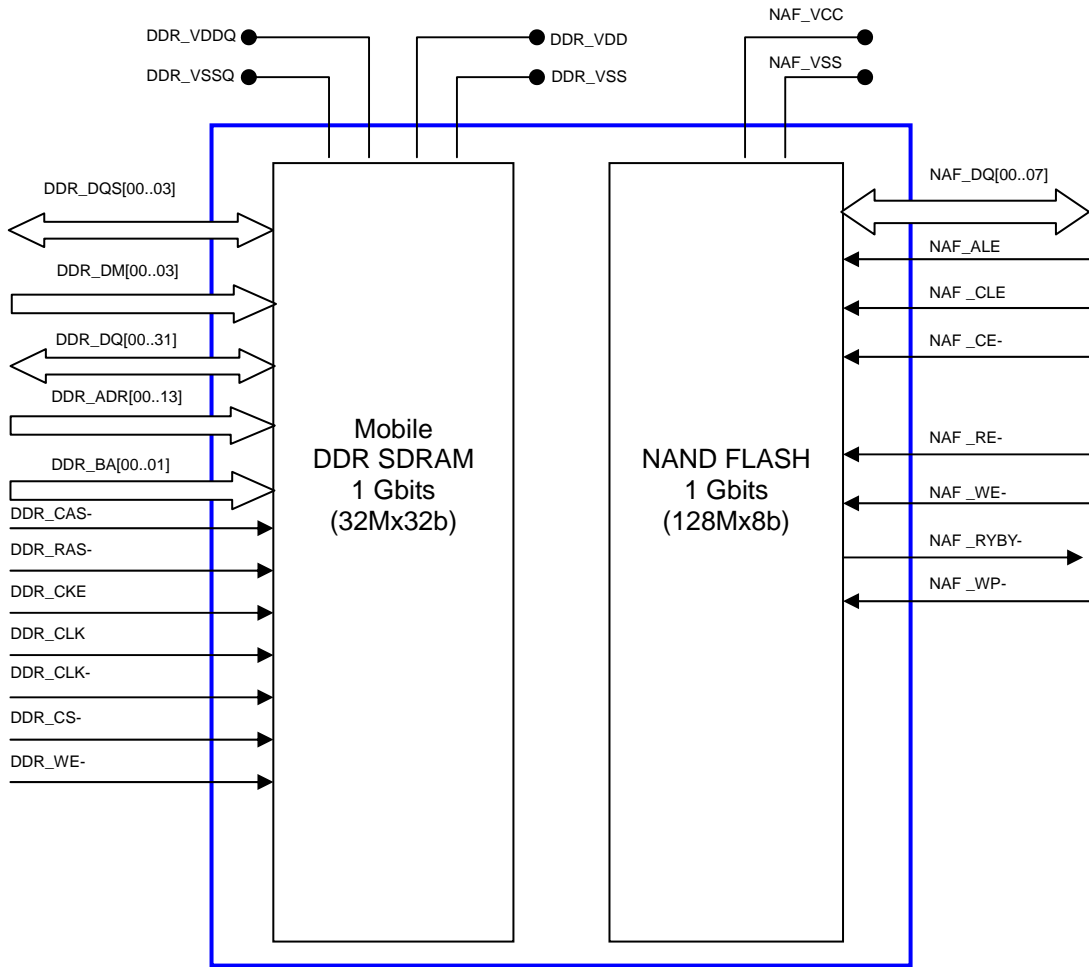
- Organization
  - Memory Cell Array : (128M+4M)x8bit.
  - Data Register : (2K+64) x 8bit
- Voltage Supply
  - 3.3V Device : 2.70V~3.60V
- Automatic Program and Erase
  - Page Program: (2K+64)Byte
  - Block Erase: (128K+4K)Byte
- Page Read Operation
  - Page Size: (2K+64)Byte
  - Random Read: 25us(Max.)
  - Serial Access: 25ns(Min.)
- Fast Write Cycle Time
  - Page Program time: 200us(Typ.)
  - Block Erase Time: 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance: 100K Program/Erase Cycles(with 1bit/512Bytes ECC)
  - Data Retention: 10Years
- Command Driven Operation
- Intelligent Copy-Back with internal 1bit/528Bytes EDC

### MOBILE DDR SDRAM Features

- Mobile DDR SDRAM
  - Double data rate architecture: two data transfer per clock cycle
- Mobile DDR SDRAM INTERFACE
  - X32 bus width
  - Multiplexed Address (Row address and Column address)
- SUPPLY VOLTAGE
  - 1.8V device: DDR\_VDD and DDR\_VDDQ=1.7V to 1.95V
- MEMORY CELL ARRAY
  - 1Gbit (x32 device)=8M x 4Bank x32 I/O
- DATA STROBE
  - X32 device: DDR\_DQS00~DDR\_DQS03
  - Bidirectional, data strobe (DDR\_DQS[00..03]) is transmitted and received with data, to be used in capturing data at the receiver
  - Data and data mask referenced to both edges of DDR\_DQS[00..03]
- LOW POWER FEATURES
  - PASR (Partial Array Self Refresh)
  - AUTO TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
  - DPD (Deep Power Down): DPD is an optional feature
- INPUT CLOCK
  - Differential clock inputs(DDR\_CLK, DDR\_CLK-)
- Data MASK
  - DDR\_DM00~DDR\_DM03:Input mask signals or write data
  - DDR\_DM[00..03] masks write data-in at the both rising and falling edges of the data strobe
- MODE REGISTER SET, EXTENDED MODE REGISTER SET and STATUS REGISTER READ
- DDR\_CAS- LATENCY
  - Programmable DDR\_CAS- latency 2 or 3 supported
- BURST LENGTH
  - Programmable burst length 2/4/8 with both sequential and interleave mode
- AUTO PRECHARGE
  - Option for each burst access
- AUTO REFRESH AND SELF REFRESH MODE
- CLOCK STOP MODE
  - Clock stop mode is a feature supported by Mobile DDR SDRAM
- INITIALIZING THE MOBILE DDR SDRAM
  - Occurring at device power up or interruption of device power

**2. FUNCTION DIAGRAM**

**2.1 MCP**



## 3. PACKAGE DIMENSION (137 Ball TFBGA, 11x13x1.2mm)

