

1. INTRODUCTION

M5E1G8566B is a Multi Chip Package Memory (MCP) that integrated 1G bits NAND Flash and 256M bits MOBILE DDR SDRAM by advanced SiP (System-in-a-Package) technology. M5E1G8566B offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

1.1 APPLICATION

- DSC
- DV
- PMP

1.2 FEATURES

PRODUCT LIST

- M5E1G8566B
 - NAND FLASH: 1G bits (128Mx8bit)
 - MOBILE DDR SDRAM: 256M bits (8M x2-Bank x 16-bit)

POWER SUPPLY

- NAND FLASH
 - 2.7 to 3.6V
- MOBILE DDR SDRAM
 - 1.8V

PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- TFBGA 9 x 10.2 x 1.2mm, 99 Balls
- Ball Pitch: 0.8 mm

Temperature

- Operating: 0 to +70 °C
- Storage: -55 to +125 °C

NAND FLASH

- Organization
 - x8 bus width.
 - Multiplexed Address/ Data
 - Pin out compatibility for all densities
- SUPPLY VOLTAGE
 - NAF_VCC = 2.7V to 3.6V
- Memory Cell Array
 - = (2K+64) Bytes x 64 Pages x 1,024 Blocks
- PAGE SIZE
 - (2K+64 spare) Bytes
- BLOCK SIZE
 - (128K + 4K spare) Bytes
- PAGE READ / PROGRAM
 - Random access: 25us (max.)
 - Sequential access: 30ns (min.)
 - Page program time: 200us (typ.)
- COPY BACKPROGRAM MODE
 - Fast page copy without external buffering
- CACHE PROGRAM
 - Internal (2048+64) Byte buffer to improve the program throughput
- FAST BLOCK ERASE
 - Block erase time: 2ms (typ.)
- ELECTRONIC SIGNATURE
 - 1st cycle: Manufacturer Code

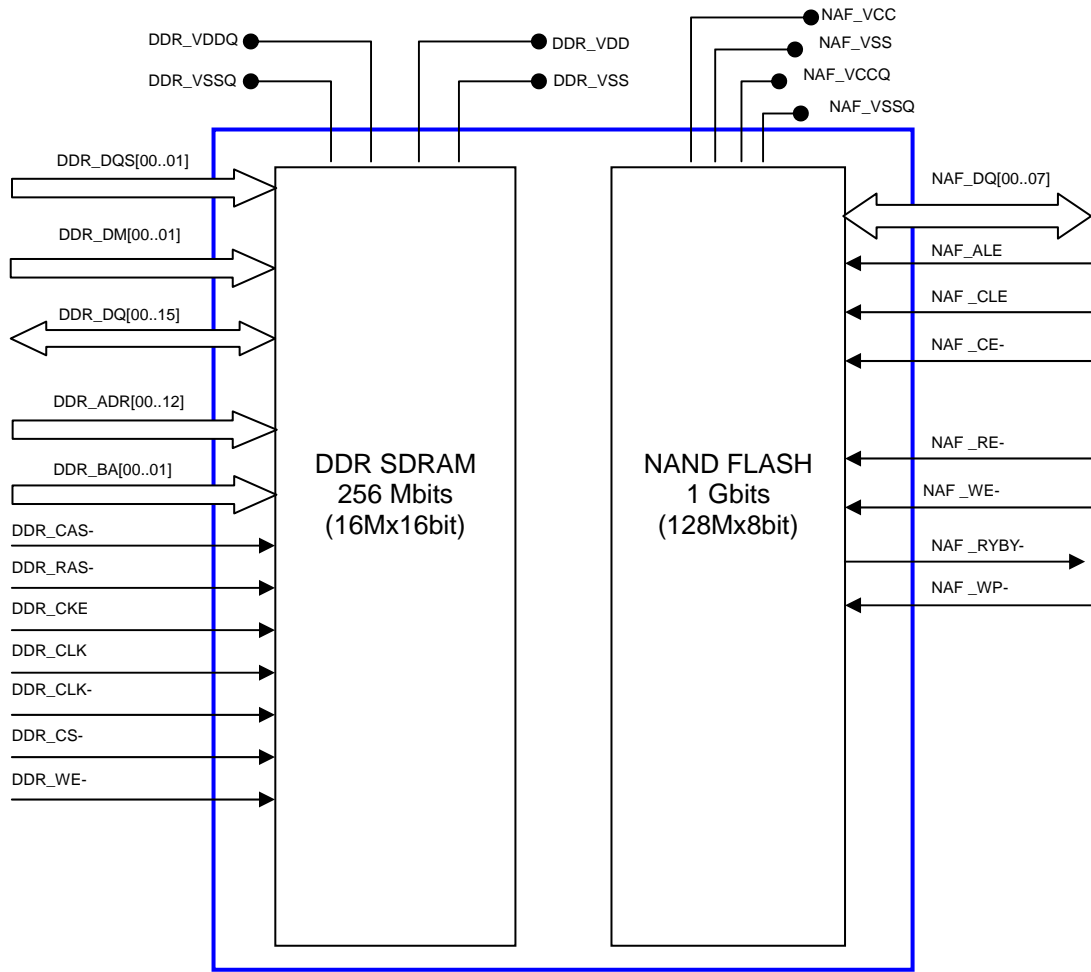
- 2nd cycle: Device Code
- 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle: Page size, Block size, Organization, Spare size
- CHIP ENABLE DON'T CARE
 - Simple interface with microcontroller
- DATA RETENTION
 - 100,000 Program/Erase cycles (with 1bit/528byte ECC)
 - 10 years Data Retention

MOBILE DDR SDRAM

- 16Mx16 Wide I/O organization
- Double data rate quad-bank synchronous DARM
- 1.8V DARM voltage
- 1.8V I/O voltage; LVTTTL
- Differential clock input (DDR_CLK and DDR_CLK-)
- Bi-directional data strobe for each data byte
- Burst Length: 2,4, and 8
- Sequential Burst only
- DDR_CAS Latency:2 and 3
- Data DDR_DQ[00..15] transactions on both edges of data strobe
- Edge aligned data output and center aligned data input
- Non-DLL operation; DDR_DQS delayed from DDR_CLK and DDR_CLK-
- Full and partial array self-refresh
- Internal temperature compensated self-refresh
- Deep power down mode
- 64ms auto-refresh period
- Selectable output drive strength
- Clock stop capability

2. FUNCTION DIAGRAM

2.1 MCP



3. PACKAGE DIMENSION (99 Ball TFBGA, 9x10.2x1.2mm)

