

1. INTRODUCTION

M5E568562B is a Multi Chip Package Memory (MCP) that integrated 256Mb bits NAND Flash and 256M bits MOBILE DDR SDRAM by advanced SiP (System-in-a-Package) technology. M5E568562B offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

1.1 APPLICATION

- Feature Phone
- Smart Phone
- MID

1.2 FEATURE

PRODUCT LIST

- M5E568562B
 - NAND FLASH: 256M bits (32Mx8-bit)
 - MOBILE DDR SDRAM: 256M bits (2Mx32-bitx4Bank)

POWER SUPPLY

- NAND FLASH
 - 2.7 to 3.6V
- MOBILE DDR SDRAM
 - 1.8V

PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- FBGA11 x 13 x 1.2mm, 137 Balls
- Ball Pitch: 0.8 mm

Temperature

- Operating: 0 to +70 °C
- Storage: -55 to +125 °C

NAND FLASH Features

- Voltage Supply
2.7 ~ 3.6 V
- Organization
 - Memory Cell Array
(32M + 1024K)bit x 8 bit
 - Data Register
(512 + 16)bit x 8bit
- Automatic Program and Erase
 - Page Program
(512 + 16)Byte
 - Block Erase :
(16K + 512)Byte
- Page Read Operation
 - Page Size
(512 + 16)Byte
 - Random Access : 15 μ s(Max.)
 - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
 - Program time : 200 μ s(Typ.)
 - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
 - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology

- Endurance : 100K Program/Erase Cycles
- Data Retention : 10 Years

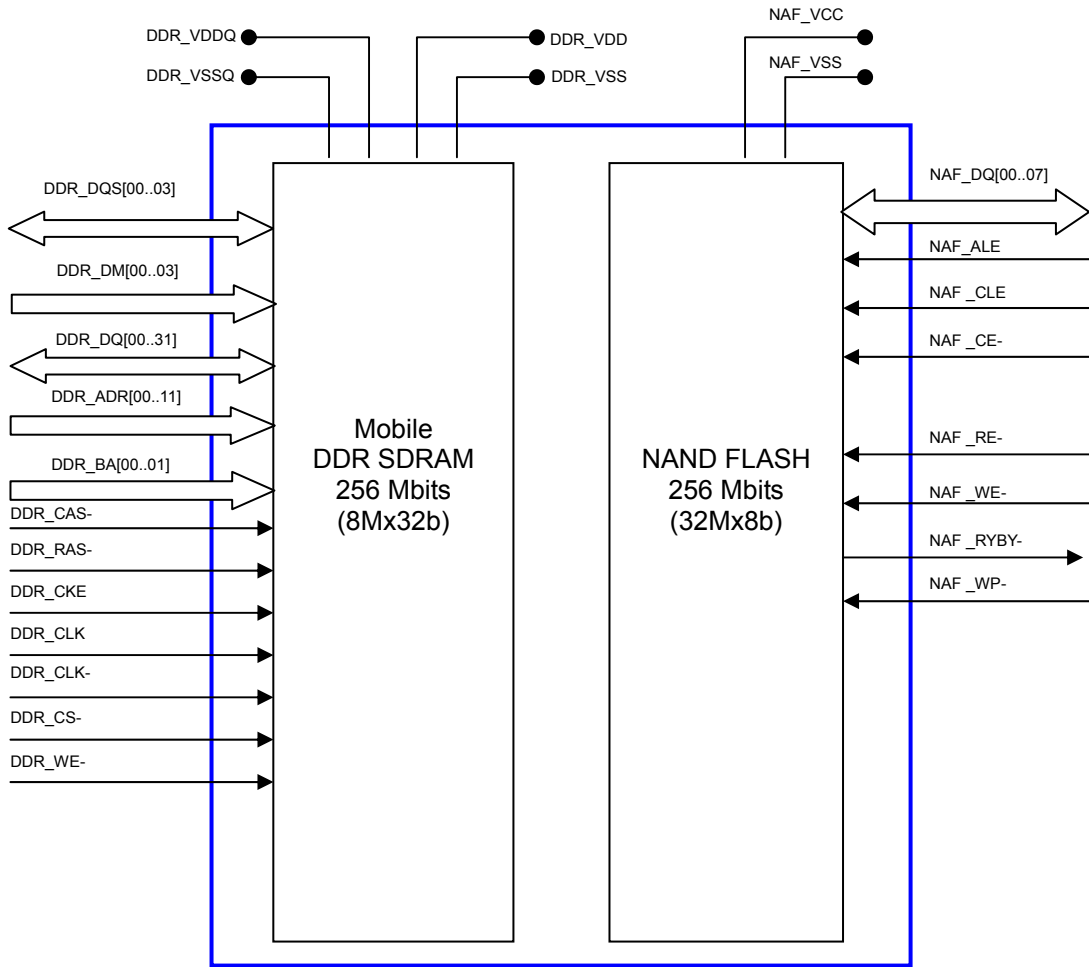
- Command Register Operation
- Intelligent Copy-Back
- Unique ID for Copyright Protection

MOBILE DDR SDRAM Features

- Double data rate architecture: two data transfer per clock cycle
- Mobile DDR SDRAM INTERFACE
 - X32 bus width
 - Multiplexed Address (Row address and Column address)
- SUPPLY VOLTAGE
 - 1.8V device: DDR_VDD and DDR_VDDQ=1.7V to 1.95V
- MEMORY CELL ARRAY
 - 256Mbit (x32 device)=2M x 4Bank x32 I/O
- DATA STROBE
 - DDR_DQS[00..03]
 - Bidirectional, data strobe (DDR_DQS[00..03]) is transmitted and received with data, to be used in capturing data at the receiver
 - Data and data mask referenced to both edges of DDR_DQS[00..03]
- LOW POWER FEATURES
 - PASR (Partial Array Self Refresh)
 - AUTO TCSR (Temperature Compensated Self Refresh)
 - DS (Drive Strength)
 - DPD (Deep Power Down): DPD is an optional feature
- INPUT CLOCK
 - Differential clock inputs(DDR_CLK, DDR_CLK-)
- Data MASK
 - DDR_DM[00..03]:Input mask signals or write data
 - DDR_DM[00..03] masks write data-in at the both rising and falling edges of the data strobe
- MODE REGISTER SET, EXTENDED MODE REGISTER SET and STATUS REGISTER READ
 - Keep to the JEDEC Standard regulation (Low Power DDR SDRAM)
- DDR_CAS- LATENCY
 - Programmable DDR_CAS- latency 2 or 3 supported
- BURST LENGTH
 - Programmable burst length 2/4/8 with both sequential and interleave mode
- AUTO PRECHARGE
 - Option for each burst access
- AUTO REFRESH AND SELF REFRESH MODE

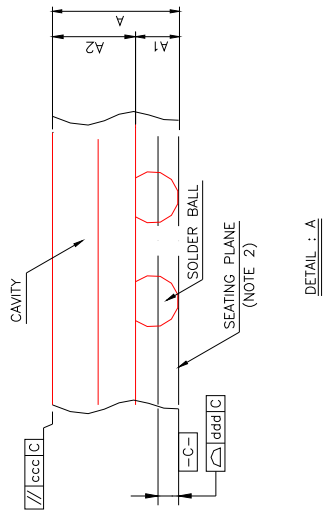
- CLOCK STOP MODE
 - Clock stop mode is a feature supported by Mobile DDR SDRAM
 - Keep to the JEDEC Standard regulation
- INITIALIZING THE MOBILE DDR SDRAM
 - Occurring at device power up or interruption of device power

2. FUNCTION DIAGRAM
2.1 MCP

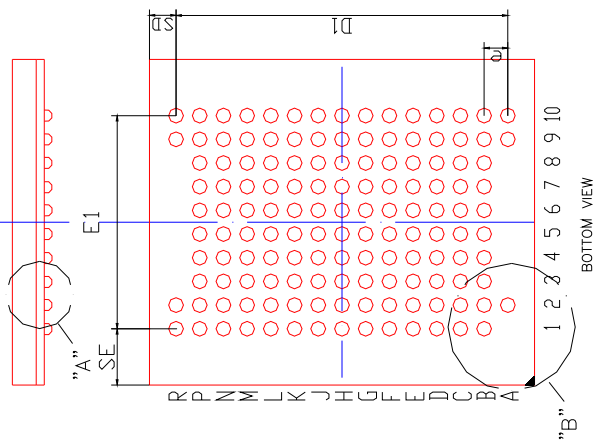
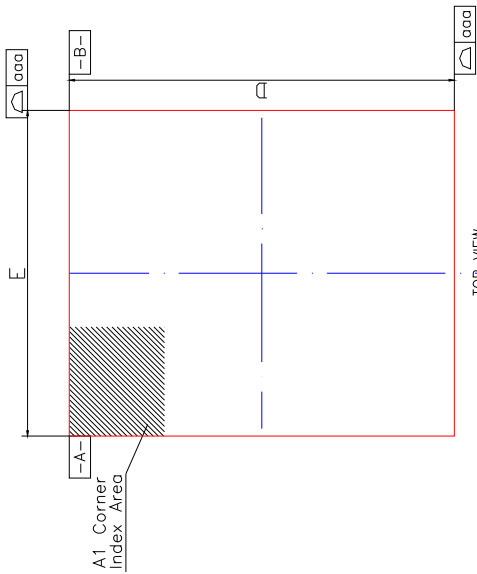
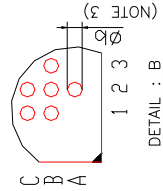
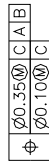


3. PACKAGE DIMENSION (137 Ball TFBGA, 11x13x1.2mm)

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	1.20	1.25
A1	0.27	0.32	0.37
A2	---	---	0.91
D	12.90	13.00	13.10
E	10.90	11.00	11.10
D1	11.10	11.20	11.30
E1	7.10	7.20	7.30
e	---	0.80	---
b	0.40	0.45	0.50
SD	---	0.90	---
SE	---	1.90	---
aaa	0.15		
ccc	0.20		
ddd	0.12		
MD/ME	15/10		



- NOTE :
1. CONTROLLING DIMENSION : mm.
 2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .



Confidential Document